OBJECTIVE ANALYSIS
Semiconductor Market Research

OBJECTIVE ANALYSIS ALERT!

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MICRON & INTEL'S 34NM 3-BIT NAND ARRIVES

Today Intel & Micron announced their introduction of a 34nm 3-bit NAND chip. This device, which stores 3 bits per cell, can pack 32Gb of data into a chip that is only 126mm².

The chip is not for all markets. Just as SLC NAND was once thought to be poorly suited to SSDs, then poorly suited to enterprise SSDs, this chip, with a very low endurance level, is currently being promoted by the companies as a device well suited to USB flash drives and flash cards for cameras and cell phones, but the companies explained that they need more experience in production volumes before they will be confident to position it as a chip suitable for the high-write environment of the SSD.

So what benefit is there in this chip?

NAND has grown faster than any market in the history of semiconductors because of its extremely fast price reductions. Although Moore's Law supports annual "per gigabyte" price reductions of around 30%, NAND has harnessed a number of techniques to race past that standard decline to cut manufacturing costs at an average rate of 40% per annum. The difference between these two rates is enormous.

One factor that has supported this high rate of decline has been the migration of NAND from SLC to MLC. That was a one-time event. Now the technology is moving to 3 bits per cell, another accelerator for price declines. Readers of our report: ***Understanding the NAND Market*** are already familiar with this approach.

Manufacturers who have the lowest cost structure are in a position to profit at prices that would cause losses to their competition. The Micron-Intel device is a move in that direction.

But Intel and Micron are not alone with this technology. SanDisk and Toshiba announced a similar product in January, with projections of shipments in the third quarter, although SanDisk's most recent teleconference indicates that the JV's 32nm 3-bit chip is now expected to begin to ship at the end of the year. Even so, this implies that Micron and Intel don't necessarily have a sustainable lead.

The companies appear to have a strong grasp of this, and spoke of their plans to move to the next process, one they call their "2xnm generation" by the end of the year. They are confident that their 3-bit technology is capable of being used at this process geometry.

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Objective Analysis expects for this chip to cause snags for the other vendors in the market: Samsung, and Hynix/Numonyx. By the first part of 2010 manufacturers with 3-bit 3xnm product will be impressively more profitable than their competition.

The NAND market continues to be a tough battlefield, and the clear advantage falls to those with the most cost-effective technology.

Jim Handy
+1 (408) 356-2549
Objective Analysis
PO Box 440
Los Gatos, CA 95031-0440
USA
www.Objective-Analysis.com

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